10/552227

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1. Your reference — PHGB 030042GBP

2. Patent application number *(The Patent Office will fill in this part)* — 0308168.4

09APR03 E798929-2 D02879
P01/7700 0.00-0308168.4

3. Full name, address and postcode of the or of each applicant (*underline all surnames*)

KONINKLIJKE PHILIPS ELECTRONICS N.V.
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THE NETHERLANDS

Patents ADP Number (*if you know it*) — 07419294001

09 APR 2003

If the applicant is a corporate body, give the country/state of its incorporation — THE NETHERLANDS

4. Title of the invention — RECEIVER HAVING DC OFFSET VOLTAGE CORRECTION

5. Name of your agent (*if you have one*)

"Address for service" in the United Kingdom to which all correspondence should be sent (*including the postcode*)

Philips Intellectual Property & Standards
Cross Oak Lane
Redhill
Surrey RH1 5HA

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Country	Priority Application number	Date of filing

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

Number of earlier application	Date of filing (*day/month/year*)

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? (*Answer "Yes" if:*

a) any applicant named in part 3 is not an inventor, or
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Description	6
Claims(s)	2
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11. I/We request the grant of a patent on the basis of this application.

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DESCRIPTION

RECEIVER HAVING DC OFFSET VOLTAGE CORRECTION

The present invention relates to a receiver having dc offset voltage correction and to method of dc offset voltage correction in a demodulated signal. The receiver may have particular, but not exclusive, application in radio systems operating in accordance with Bluetooth™

The problem of unwanted dc offsets in radio receivers is well known and there have been many proposals for overcoming it. Patent Specification WO 02/54692 (Applicant's reference PHGB 010002) discloses a receiver having a variable threshold slicer circuit. Figure 7 of this Specification shows an embodiment of a receiver in which provision is made for correcting for dc offset voltage so that data in a demodulated signal can be detected more accurately by slicing the signal. The dc offset voltage is initially estimated by applying the demodulated input signal to a first input of a differencing stage. A default value of a selected threshold voltage is applied to a second input of the differencing circuit and an output voltage comprising a dc offset voltage estimate plus noise is obtained. This output voltage is applied to an averaging circuit in which the voltage is averaged over a period corresponding to say 25 bit periods. A low pass filter filters the output of the averaging circuit to remove the noise and the result is stored as the dc offset voltage. In operation the stored dc offset voltage is subtracted from a selected threshold circuit to be used by a bit slicer and the difference voltage acts as a modified threshold voltage which is used by a bit slicer for slicing the demodulated voltage. Whilst this circuit functions satisfactorily it is desired that a dc offset circuit operating at frequencies used by systems such as Bluetooth™ should be more responsive.

Other techniques for compensating for dc offset voltage, base line wander and level correction all associated with unwanted disturbing influences on the signal transmission path are disclosed in US Patent Specifications 6,324,231 B1 and 6,175,728 B1, EP-A2-928215 and EP-B1-16503.

Some methods of dc offset voltage compensation are unable to be fully effective when there a long sequences of unvarying data such as 1s or 0s.

An object of the present invention is to prevent long sequences of non-varying data from affecting the dc offset voltage estimate and to make the offset estimate responsive to frequency drift.

According to a first aspect of the present invention there is provided a receiver comprising means for demodulating a received signal to produce an uncorrected demodulated signal, a dc offset voltage correcting circuit having an output for a corrected signal and a data recovery circuit coupled to the output, the dc offset voltage correcting circuit comprising an input for the uncorrected demodulated signal, a bit slicer for detecting received data, filtering means for regenerating the demodulated signal less noise and dc offset, subtracting means for subtracting the regenerated demodulated signal from the uncorrected demodulated signal to produce the dc offset voltage and a feedback circuit for feeding back the dc offset voltage to the bit slicer.

According to a second aspect of the present invention there is provided a method of dc offset voltage correction in a demodulated signal, comprising obtaining a dc free estimate of the demodulated signal, subtracting the dc free estimate of the demodulated signal from a contemporaneous version of the demodulated signal to obtain a dc offset voltage and subtracting the dc offset voltage from the demodulated signal.

The present invention is based on the concept that removing the effect of the demodulated signal from an input signal will provide an estimate of the dc offset voltage. This estimate can be subtracted from the input signal to provide a signal in which data can be detected accurately by slicing. This architecture has the advantage of preventing long sequences of non-varying data from affecting the dc offset voltage estimate and of making the offset estimate responsive to frequency drift by avoiding the use of filters having relatively long time constants.

A level correction circuit architecture disclosed in EP-B1-16503 is concerned with correcting the level of television teletext signals and differs

from that used in the receiver circuit made in accordance with the present invention in that a waveform corrected signal is derived from a bit slicer coupled to an output of a level correcting circuit. Additionally the waveform corrected signal is applied to an amplitude control circuit for the correction of the "a" level corresponding to a logic one level in the television signal and it is the output from this circuit which is subtracted from an input signal to obtain an error signal. The error signal is integrated in an integrating circuit to produce a level control signal which is supplied to the level correcting circuit. The amplitude control signal corresponding to the level "a" is derived from the input signal by obtaining the difference between a logic zero level which corresponds to the black level "b" and the logic one value corresponding with a level "(b + a)" in the television signal. The levels "b" and "(b + a)" can show variations caused by disturbing influences on the transmission path. This cited circuit is not concerned with overcoming the effects of unwanted dc offset voltages. The receiver circuit made in accordance with the present invention does not need an amplitude control circuit for signal level control between two logic levels.

The present invention will now be described, by way of example, with reference to the accompanying drawings, wherein:

Figure 1 is a block schematic diagram of an embodiment of a radio receiver made in accordance with the present invention,

Figure 2 illustrates a data signal in a simulated Bluetooth™ system,

Figure 3 illustrates is a demodulated verision of the data signal shown in Figure 2,

Figure 4 illustrates a dc estimate obtained using the dc offset voltage circuit included in the receiver shown in Figure 1, and

Figures 5 and 6, for the sake of comparison only, respectively illustrate dc offset voltage estimates obtained using a simulated "MaxMin" circuit and a simulated 10kHz bandwidth low pass filter.

Referring to Figure 1, the illustrated radio receiver comprises an antenna 10 for receiving for example a Bluetooth™ signal which may comprise random data as well as long sequences of non-varying data, viz long sequences of ones or zeroes. The received signal is amplified in a rf amplifier 12 and the amplified signal is applied to a frequency down-conversion stage 14. The frequency down conversion stage 14 comprises a mixer (or multiplier) 16 having a first input coupled to an output of the rf amplifier 12 and a second input coupled to a local oscillator signal generating means 18, for example a frequency synthesizer. A bandpass filter 20 is coupled to an output of the frequency down-conversion stage 14 to select an uncorrected demodulated signal v_{in} which includes a dc offset voltage and noise.

The uncorrected demodulated signal v_{in} is supplied to a dc offset voltage correction circuit 22. Waveform diagrams have been provided to facilitate an understanding of the operation of the dc offset voltage correction circuit 22. The circuit 22 comprises a first subtracting stage 24 having a first input 25 for the uncorrected demodulated signal v_{in}, a second input 26 for a dc offset voltage v_{off} recovered by the circuit and an output 27. The signal on the output 27 is the uncorrected demodulated signal minus dc offset voltage, (v_{in} - v_{off}), which is supplied to a bit slicer 30 and by way of a line 28 to a data recovery stage 42. The output of the bit slicer 30 comprises an estimate of the demodulated signal and this signal is supplied to a low pass filter 32 which produces a dc free estimate of the demodulated signal. The low pass filter 32 has a characteristic which approximates to the transfer function of the transmit bit shaping filter and the complete receive train including for example a channel filter and the demodulator. In the case of a Bluetooth™ system the low pass filter 32 could be modelled as a 300kHz bandwidth 5^{th} order Tchebycheff 0.5dB filter.

A second subtracting stage 34 has a first input 35 coupled to an output of the low pass filter 32, a second input 36 coupled to a time delay stage 38 for delaying the uncorrected demodulated signal v_{in} by a time corresponding to the propagation of the signal through the circuit stages 24, 30 and 32, and an output. The output signal from the second subtracting stage 34 is the

contemporaneous dc offset voltage plus noise. The noise is removed using a low pass filter 40 to provide the dc offset voltage v_{off} which is fed back to the first input 26 of the first subtracting stage 24. The time constant of the low pass filter 40 should be made as short as practically possible.

In implementing the dc offset voltage correction circuit 22 the performance can be enhanced by use of an intelligent bit slicer 30 and by using a variable bandwidth filter controlled by the estimated rate of drift in place of the low pass filter 40.

The performance improvement of this method of correcting for dc offset voltages becomes particularly apparent when data is not entirely random but contains long sequences of non-varying data as shown in Figures 2 to 4. More particularly Figures 2 to 4 show simulation results for a Bluetooth™ system. A fixed DC error of 0.03 has been applied, which is equivalent to about 100kHz error. Figure 2 shows the data, Figure 3 shows the demodulated signal, and Figure 4 shows the dc offset voltage estimation.

For the sake of comparison only, Figures 5 and 6 respectively illustrate the results of simulating signal cancellation feedback dc offset estimations using the so-called "MaxMin" circuit in which the dc offset voltage is the average of maxima and minima of the signal and a conventional integration technique using a 10kHz bandwidth low pass filter. Although the relative performance of these techniques depends on the optimisation of the filters it is clearly evident that the "MaxMin" circuit is particularly inferior when used with long sequences of non-varying data and, although the integration technique is better, it is still inferior to the results obtained using the described dc offset voltage correction circuit.

Although the present invention has been described with reference to a receiver having dc offset voltage correction, the teachings of the present invention may be applied to automatic frequency control (AFC) subject to the dc offset voltage estimation being more rapid than the delay through the receiver and the AFC loop thereby avoiding introducing unwanted oscillation.

In the present specification and claims the word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. Further,

the word "comprising" does not exclude the presence of other elements or steps than those listed.

From reading the present disclosure, other modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the design, manufacture and use of radio receivers and component parts therefor and which may be used instead of or in addition to features already described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of the disclosure of the present application also includes any novel feature or any novel combination of features disclosed herein either explicitly or implicitly or any generalisation thereof, whether or not it relates to the same invention as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as does the present invention. The applicants hereby give notice that new claims may be formulated to such features and/or combinations of such features during the prosecution of the present application or of any further application derived therefrom.

CLAIMS

1. A receiver comprising means (14) for demodulating a received signal to produce an uncorrected demodulated signal, a dc offset voltage correcting circuit (22) having an output (28) for a corrected signal and a data recovery circuit (42) coupled to the output, the dc offset voltage correcting circuit (22) comprising an input for the uncorrected demodulated signal (v_{in}), a bit slicer (30) for detecting received data, filtering means (32) for regenerating the demodulated signal less noise and dc offset, subtracting means (34) for subtracting the regenerated demodulated signal from the uncorrected demodulated signal to produce the dc offset voltage (v_{off}) and a feedback circuit for feeding back the dc offset voltage to the bit slicer.

2. A receiver as claimed in claim 1, characterised in that the filtering means (32) is a low pass filter having a characteristic substantially the same as the transfer function of at least the complete receiver chain.

3. A receiver as claimed in claim 2, characterised by delay means (38) for delaying the uncorrected demodulated signal by at least the duration of the time delay due to the transmission of a signal through the filtering means.

4. A receiver as claimed in any one of claims 1 to 3, characterised in that the feedback circuit includes a low pass filter (40).

5. A receiver as claimed in any one of claims 1 to 3, characterised in that the feedback circuit includes a variable bandwidth filter controlled by the estimated rate of drift.

6. A receiver as claimed in any one of claims 1 to 5, characterised by another subtracting stage (24) having a first input (25) for the uncorrected demodulated signal (v_{in}) and a second input (26) for the dc offset voltage (v_{off})

and an output (27) coupled to the bit slicer (30) and to the data recovery circuit (42).

7. A method of dc offset voltage correction in a demodulated signal, comprising obtaining a dc free estimate of the demodulated signal, subtracting the dc free estimate of the demodulated signal from a substantially contemporaneous version of the demodulated signal to obtain a dc offset voltage and subtracting the dc offset voltage from the demodulated signal.

8. A method as claimed in claim 7, characterised by bit slicing a difference signal formed by subtracting the dc offset voltage from the demodulated signal to provide an estimate of the demodulated signal and by filtering the estimate of the demodulated signal to obtain a dc free estimate of the demodulated signal.

9. A method as claimed in claim 7 or 8, characterised by filtering the dc offset voltage.

10. A method as claimed in claim 7, 8 or 9, characterised by delaying the demodulating signal prior to subtracting the dc free estimate of the demodulated signal.

11. A receiver constructed and arranged to operate substantially as hereinbefore described with reference to and as shown in the accompanying drawings.

12. A method of dc offset voltage correction in a demodulated signal, substantially as hereinbefore described with reference to the accompanying drawings.

ABSTRACT

RECEIVER HAVING DC OFFSET VOLTAGE CORRECTION

A receiver comprises a frequency down-conversion stage (14) for demodulating a received signal to produce an uncorrected demodulated signal (v_{in}), a dc offset voltage correcting circuit (22) having an output (28) for a corrected signal and a data recovery circuit (42) coupled to the output. The dc offset voltage correcting circuit (22) comprises an input for the uncorrected demodulated signal (v_{in}), a bit slicer (30) for detecting received data, a filter (32) coupled to the output of the bit slicer for regenerating the demodulated signal less noise and dc offset, a subtracting stage (34) for subtracting the regenerated demodulated signal from a delayed version of the uncorrected demodulated signal to produce the dc offset voltage (v_{off}) and a feedback circuit for feeding back the dc offset voltage to the bit slicer.

(Figure 1)

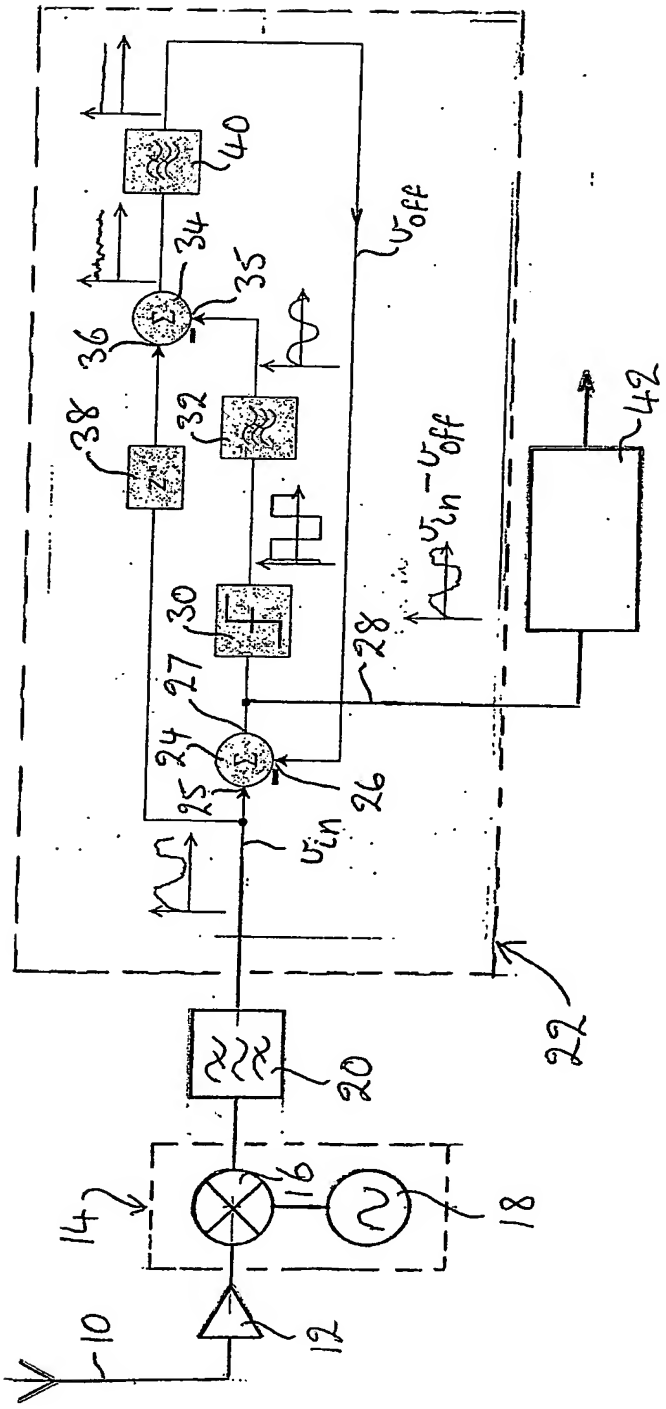

Fig. 1

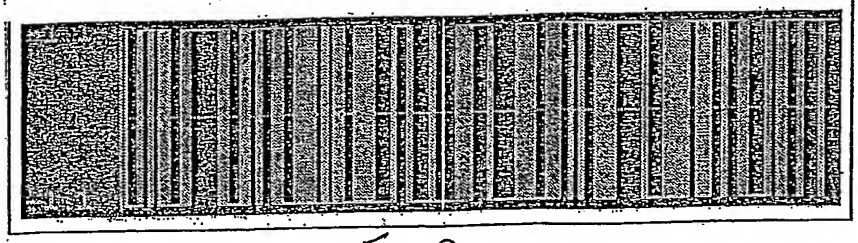

Fig. 2

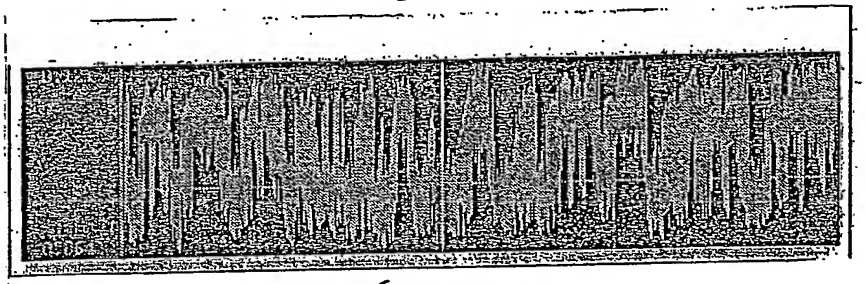

Fig. 3

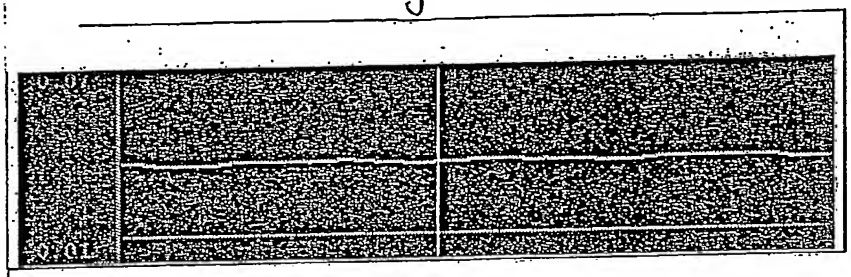

Fig. 4

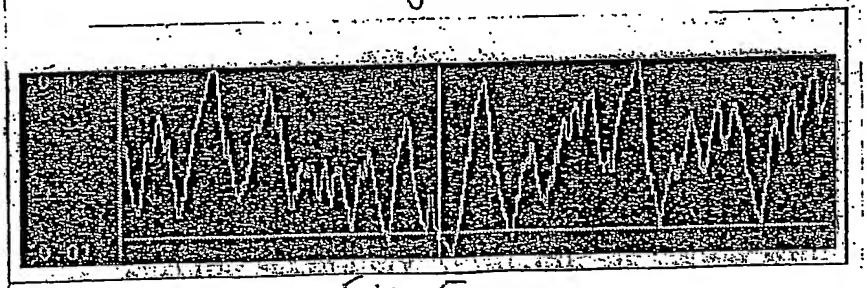

Fig. 5

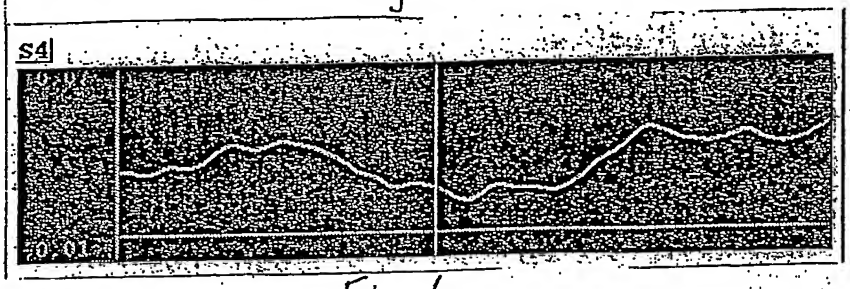

Fig. 6